

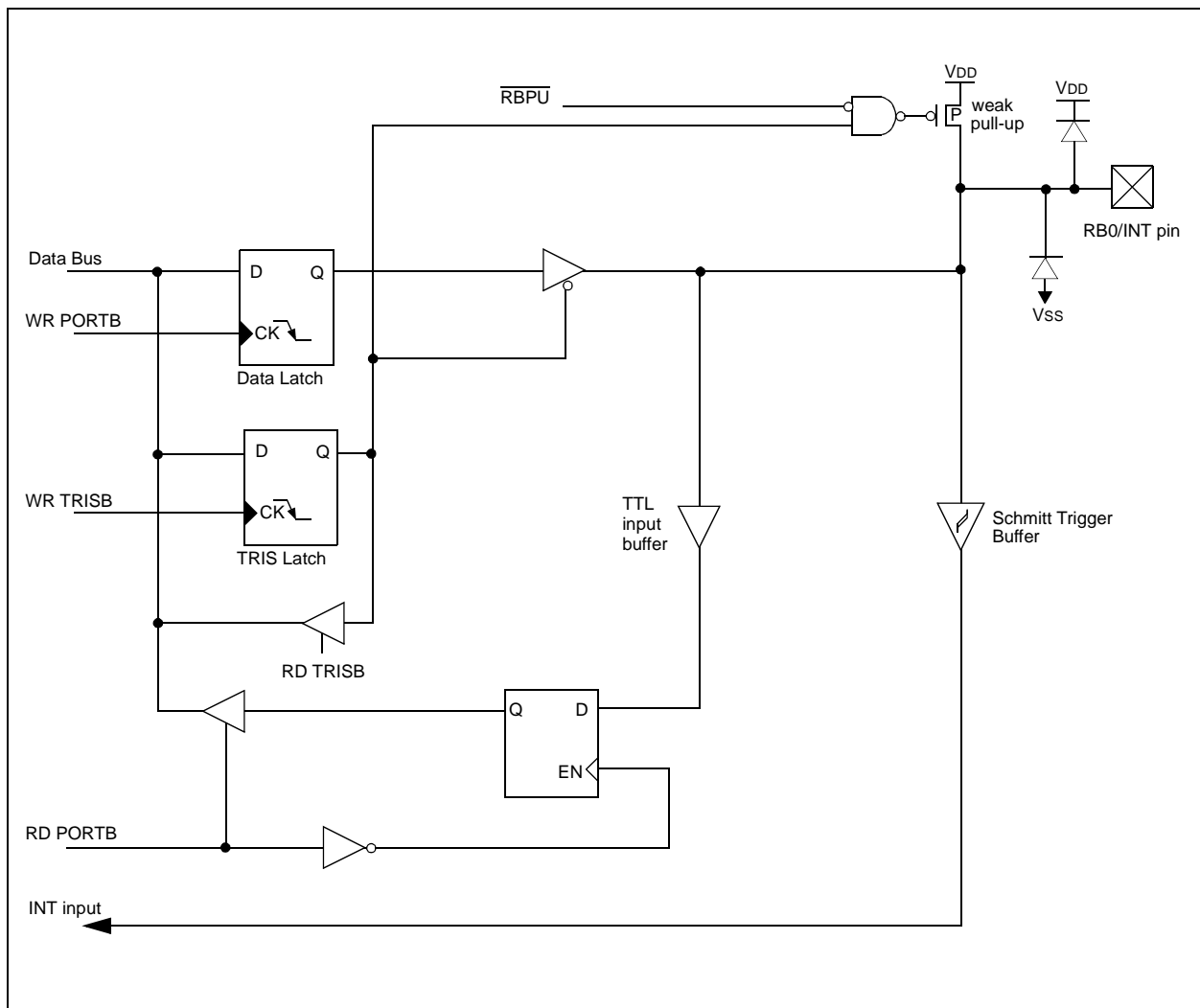
## PIC16F627 Rev. A Silicon Errata Sheet

The PIC16F627 (Rev. A) parts you have received conform functionally to the Device Data Sheet (DS40300B), except for the anomalies described below.

1. Module: I/O Ports

A read of the PORTB Data Direction Register (TRISB) returns the Data Direction state on the port pins themselves and not the contents of the TRISB register latch.

**FIGURE 1: BLOCK DIAGRAM OF RB0/INT PIN**



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**FIGURE 2: BLOCK DIAGRAM OF RB1/TX/DT PIN**

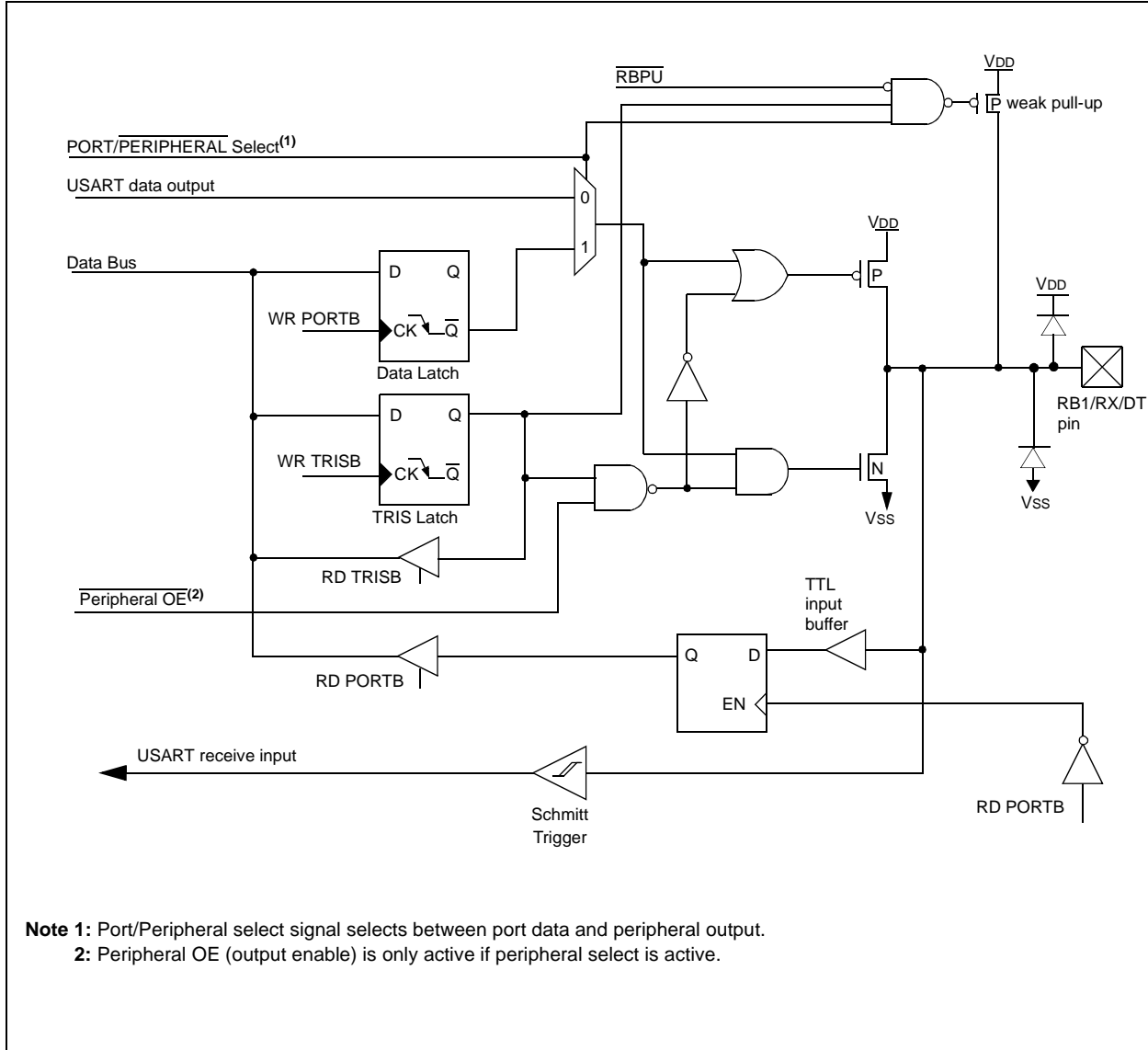
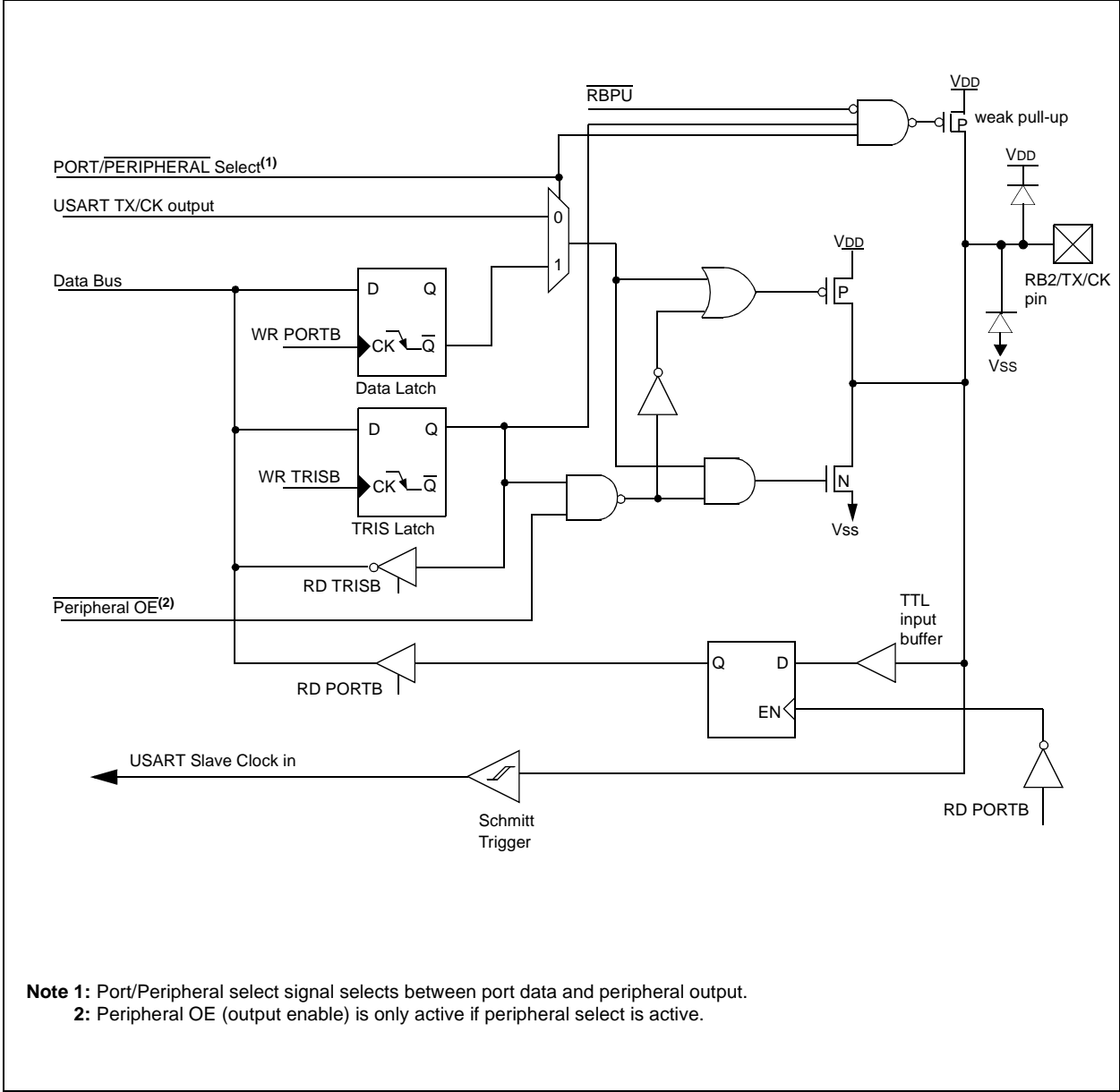


FIGURE 3: BLOCK DIAGRAM OF RB2/TX/CK PIN



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**FIGURE 4: BLOCK DIAGRAM OF THE RB3/CCP1 PIN**

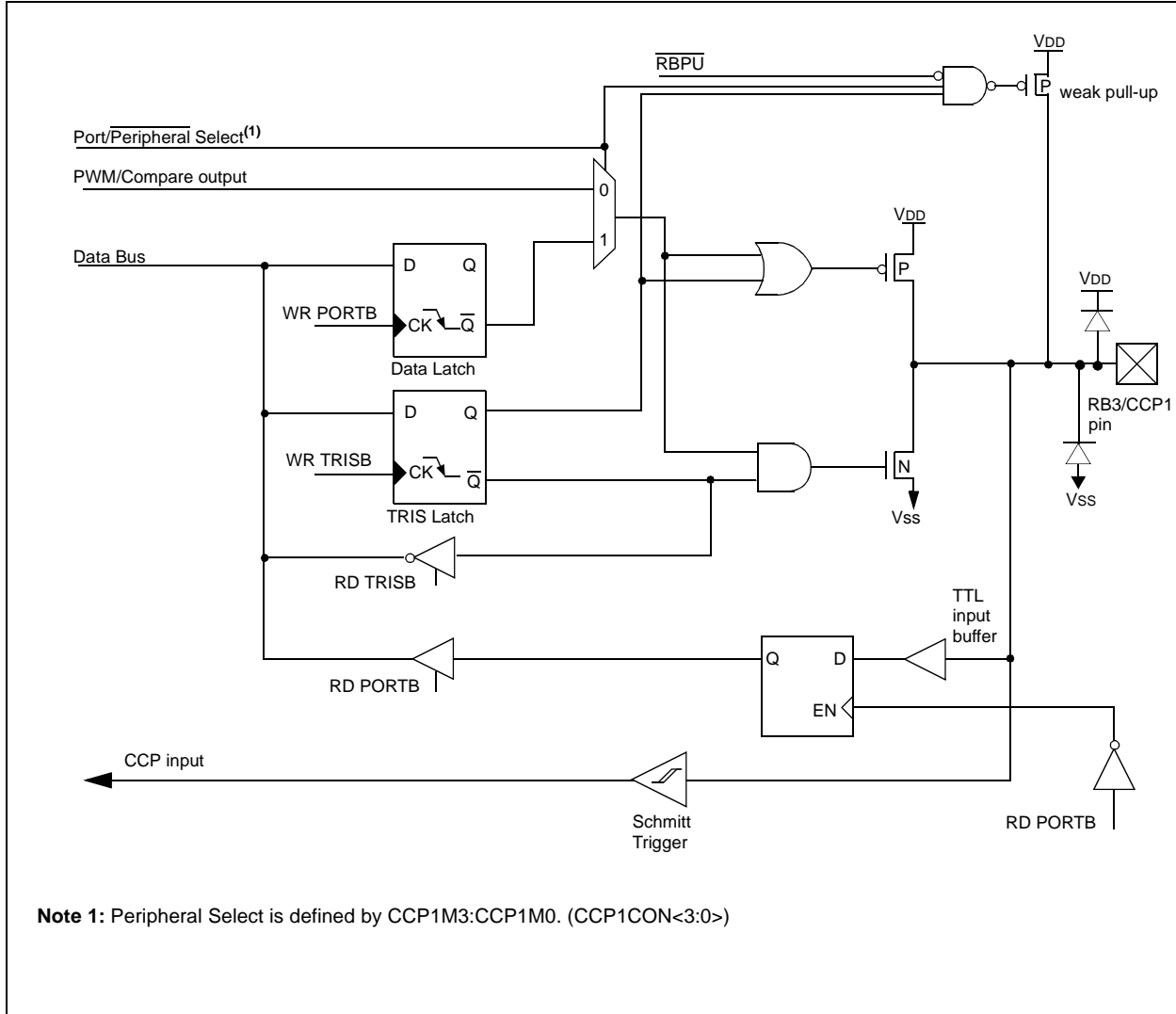
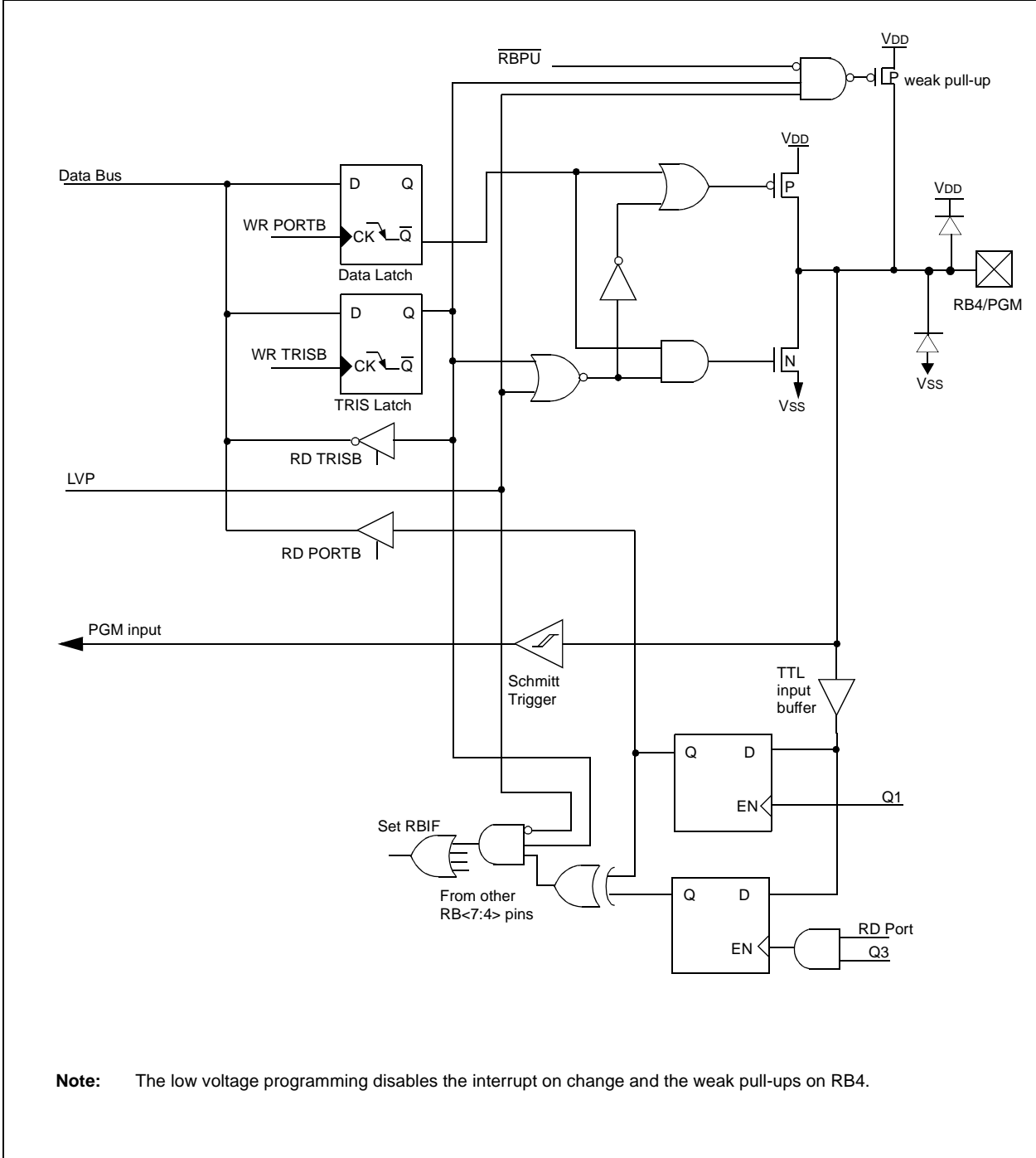


FIGURE 5: BLOCK DIAGRAM OF RB4/PGM PIN



**Note:** The low voltage programming disables the interrupt on change and the weak pull-ups on RB4.

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FIGURE 6: BLOCK DIAGRAM OF RB5 PIN

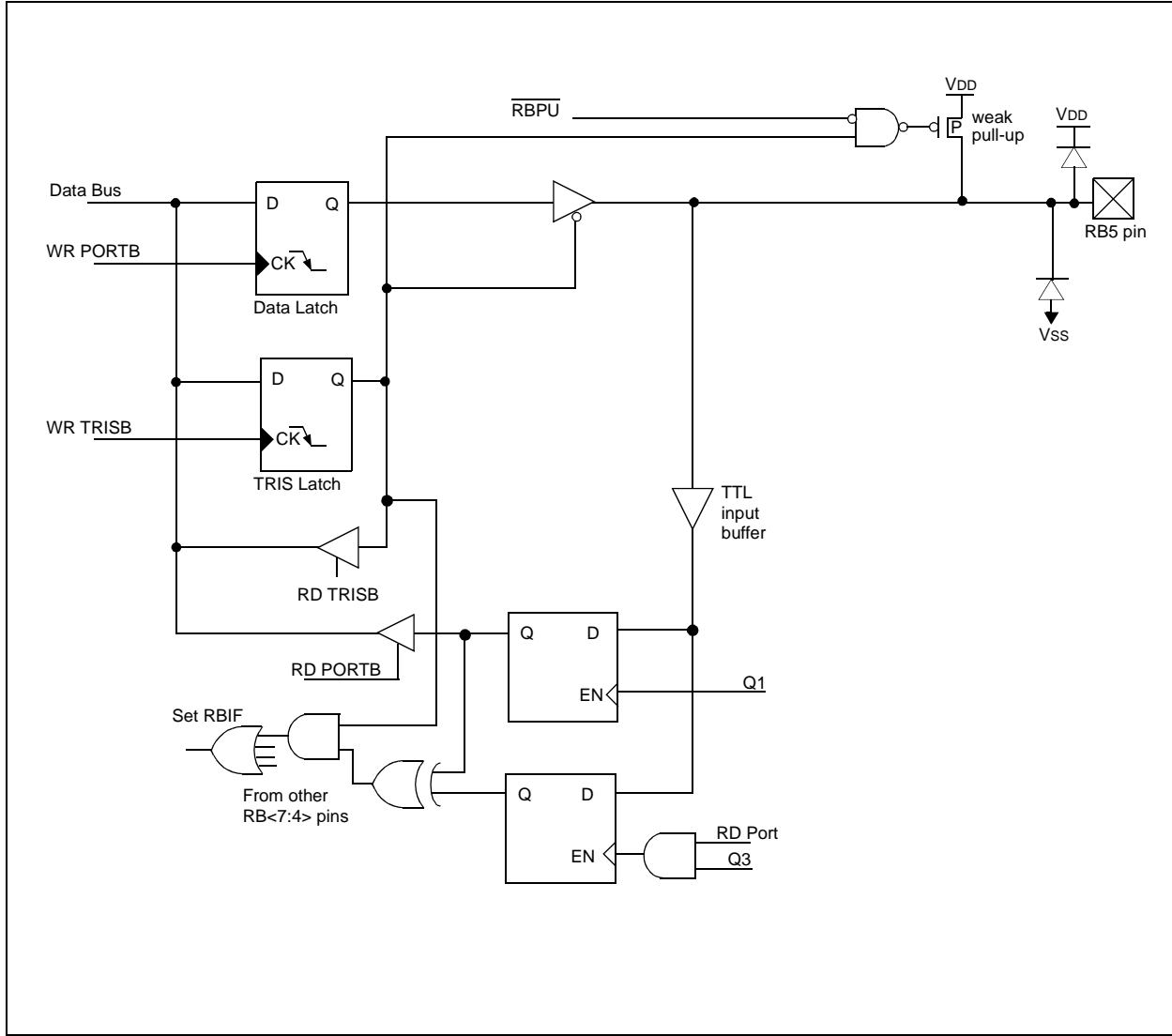
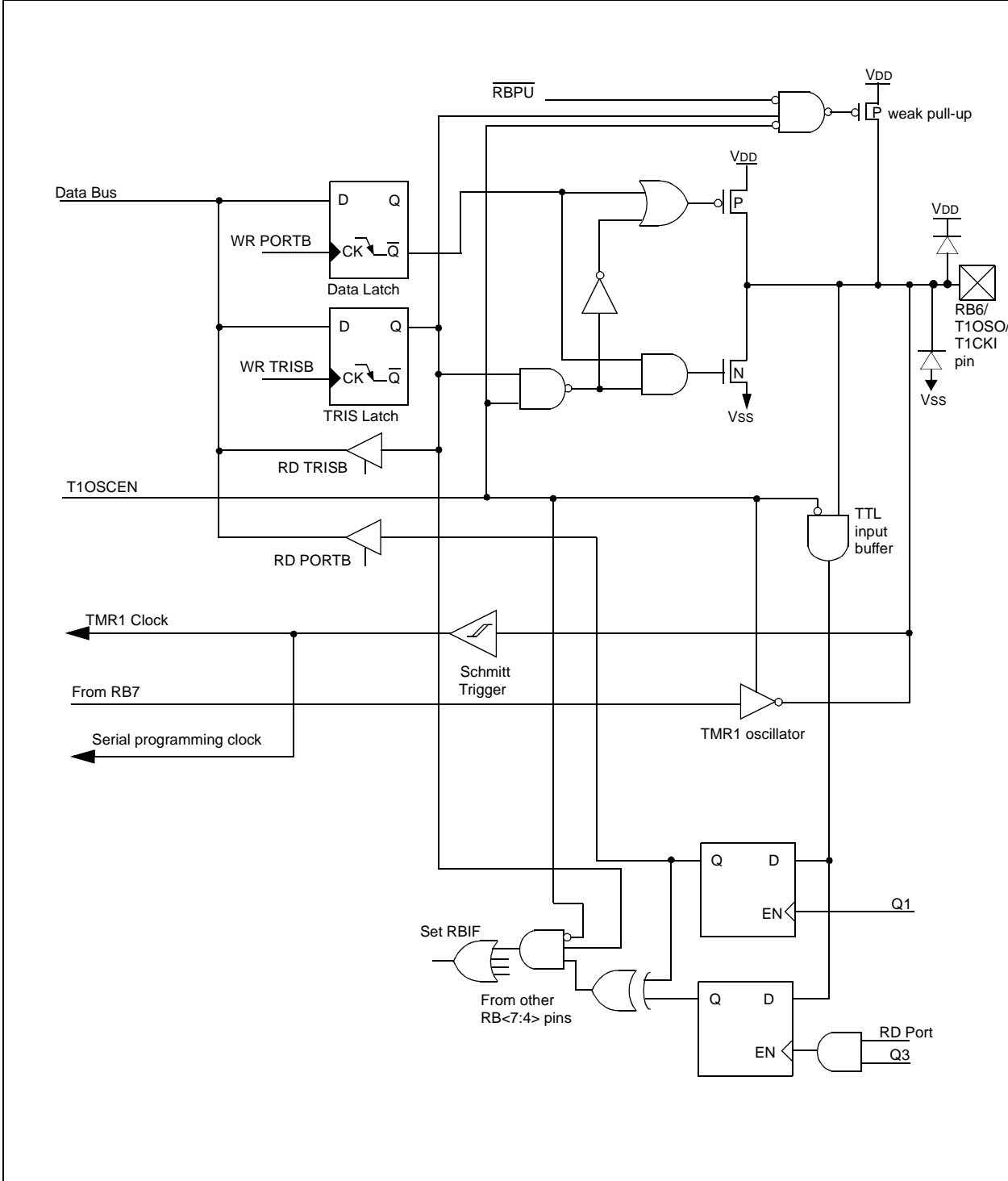
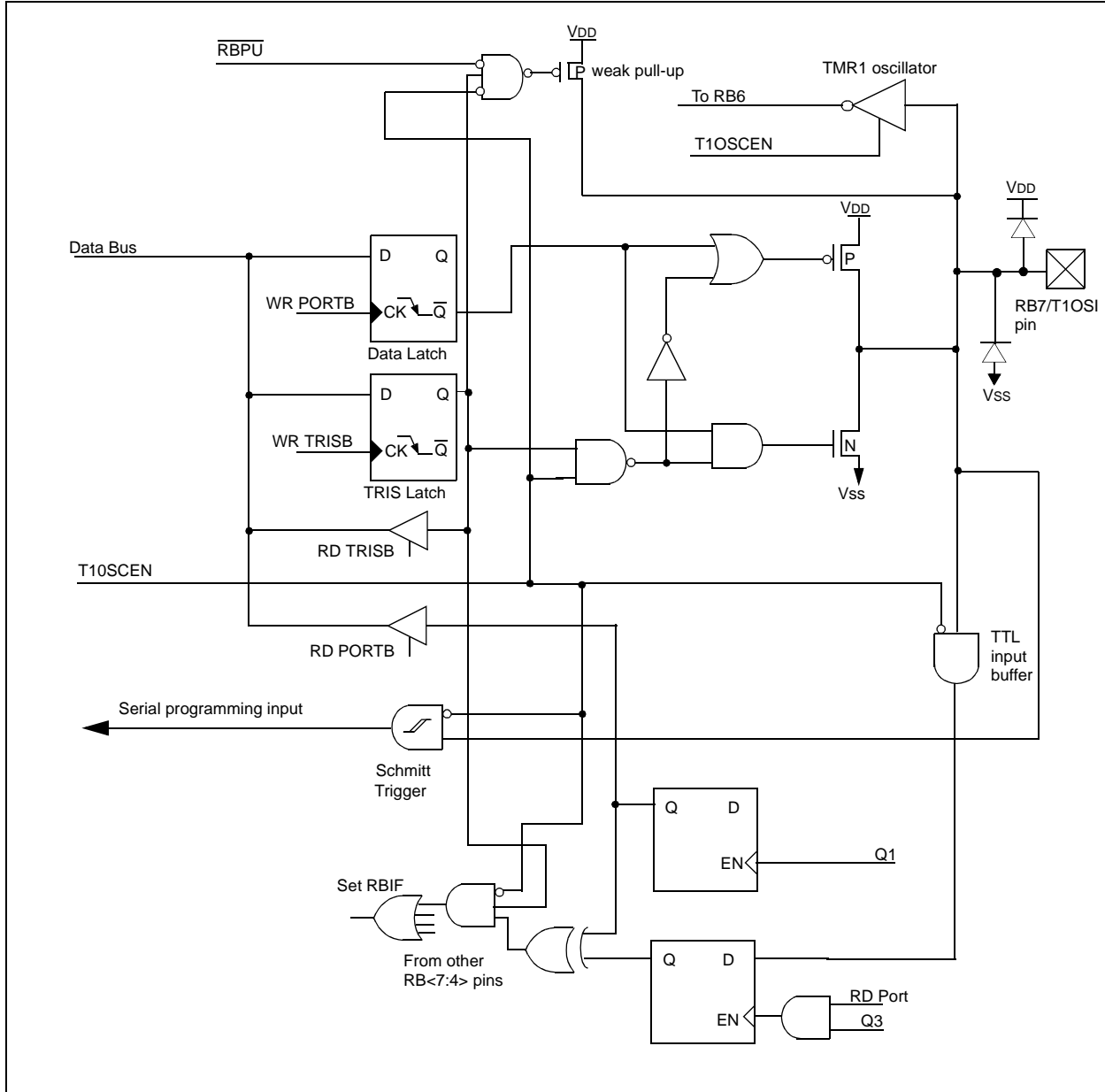


FIGURE 7: BLOCK DIAGRAM OF RB6/T1OSO/T1CKI PIN



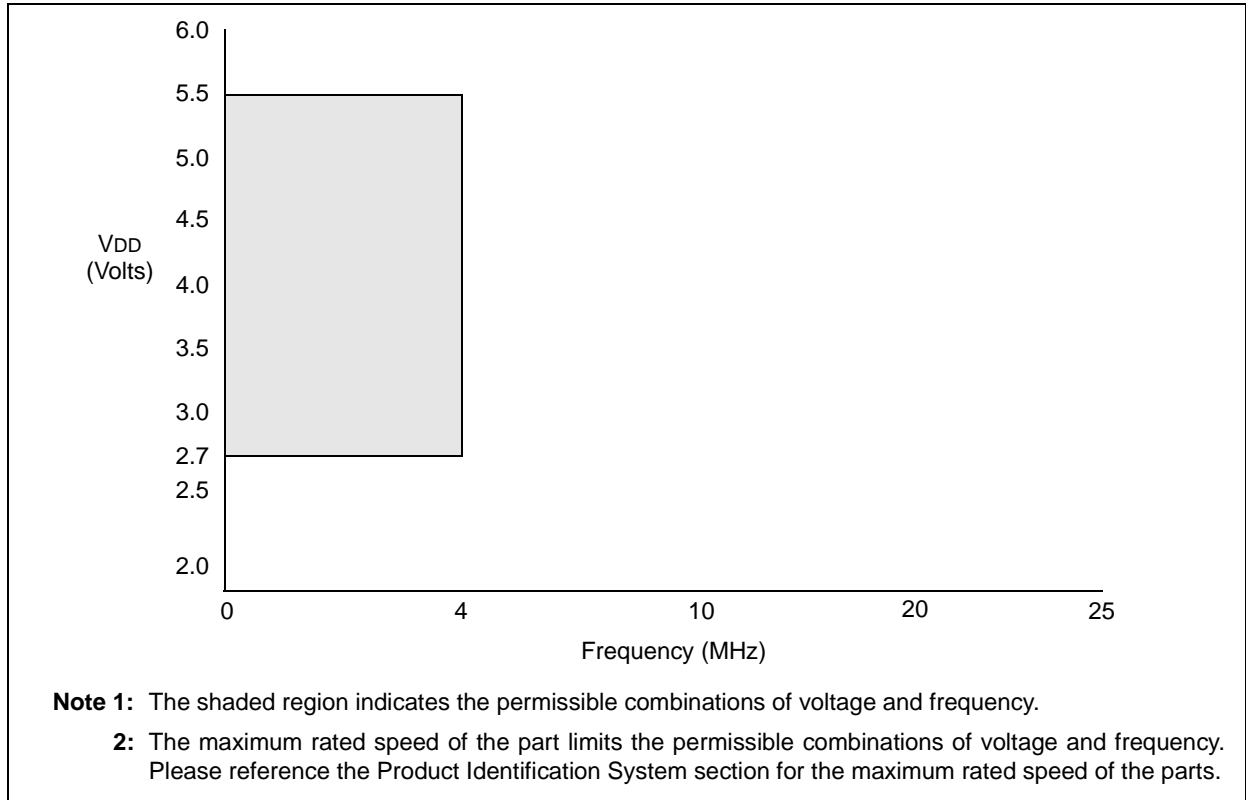
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FIGURE 8: BLOCK DIAGRAM OF THE RB7/T1OSI PIN





**FIGURE 9: PIC16LF627 VOLTAGE-FREQUENCY GRAPH,  $-40^{\circ}\text{C} \leq T_A \leq 0^{\circ}\text{C}$**



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## Clarifications/Corrections to the Data Sheet:

In the Device Data Sheet (DS40300B), the following clarifications and corrections should be noted.

1. The bit T1SYNC in the Register T1CON (address 10h) should be asserted logic low (ie.,  $\overline{T1SYNC}$ . Table 4-1, page 15, and Table 10-2, page 65, of DS40300B should be listed as follows:
2. The bit ADEN in Register RCSTA (address 18h), Table 4-1, is misspelled. The correct spelling should be ADDEN. This also appears in Figures and text on pages 72, 79, 80, 81, 82, 83, 84, 85, 86 and 89.

**TABLE 4-1: SPECIAL REGISTERS SUMMARY BANK0**

| Address       | Name  | Bit 7 | Bit 6 | Bit 5   | Bit 4   | Bit 3   | Bit 2               | Bit 1  | Bit 0  | Value on POR Reset | Value on all other Resets <sup>(1)</sup> |
|---------------|-------|-------|-------|---------|---------|---------|---------------------|--------|--------|--------------------|--|
| <b>Bank 0</b> |       |       |       |         |         |         |                     |        |        |                    |  |
| 10h           | T1CON | —     | —     | T1CKPS1 | T1CKPS0 | T1OSCEN | $\overline{T1SYNC}$ | TMR1CS | TMR1ON | --00 0000          | --uu uuuu                                |
| 18h           | RCSTA | SPEN  | RX9   | SREN    | CREN    | ADEN    | FERR                | OERR   | RX9D   | 0000 -00x          | 0000 -00x                                |

Legend: — = Unimplemented locations read as '0', u = unchanged, x = unknown, q = value depends on condition, shaded = unimplemented

**Note 1:** Other (non power-up) resets include  $\overline{MCLR}$  Reset, Brown-out Detect and Watchdog Timer Reset during normal operation.

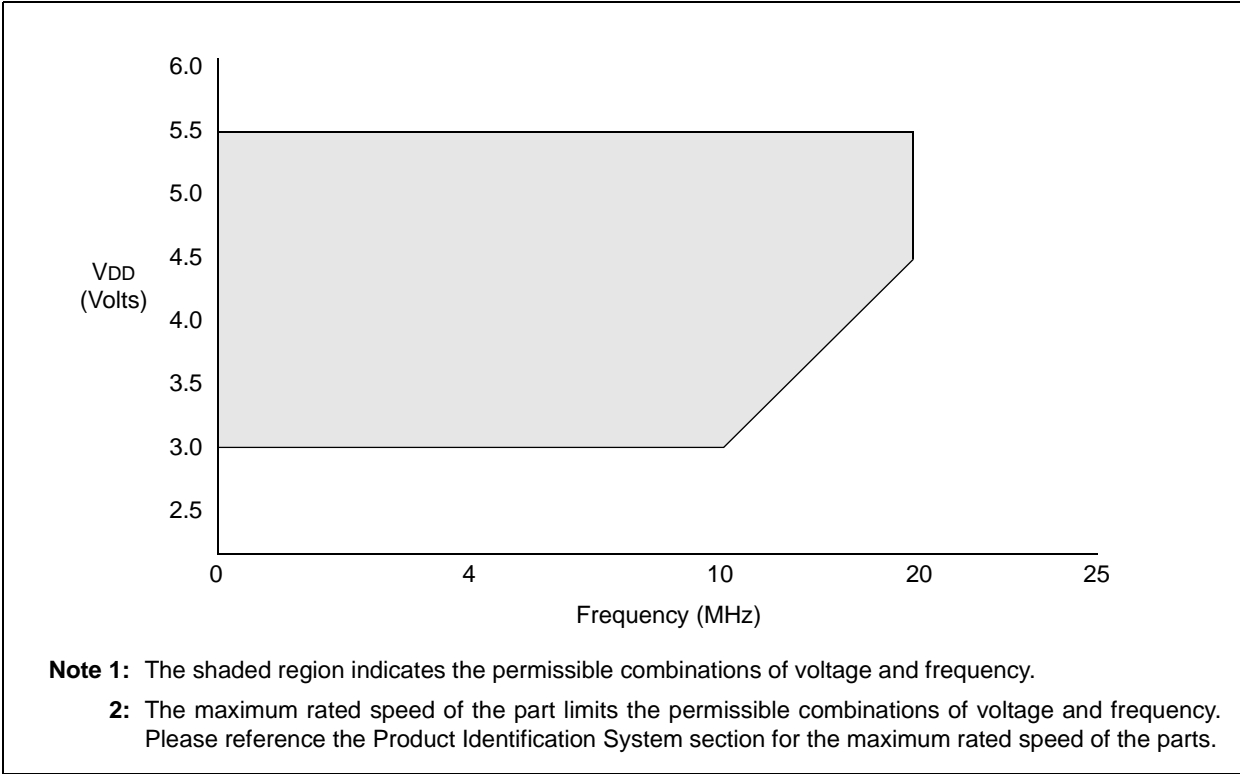
**TABLE 10-2 REGISTERS ASSOCIATED WITH CAPTURE, COMPARE, AND TIMER1**

| Address | Name  | Bit 7 | Bit 6 | Bit 5   | Bit 4   | Bit 3   | Bit 2               | Bit 1  | Bit 0  | Value on POR | Value on all other resets |
|---------|-------|-------|-------|---------|---------|---------|---------------------|--------|--------|--------------|---------------------------|
| 10h     | T1CON | —     | —     | T1CKPS1 | T1CKPS0 | T1OSCEN | $\overline{T1SYNC}$ | TMR1CS | TMR1ON | --00 0000    | --uu uuuu                 |

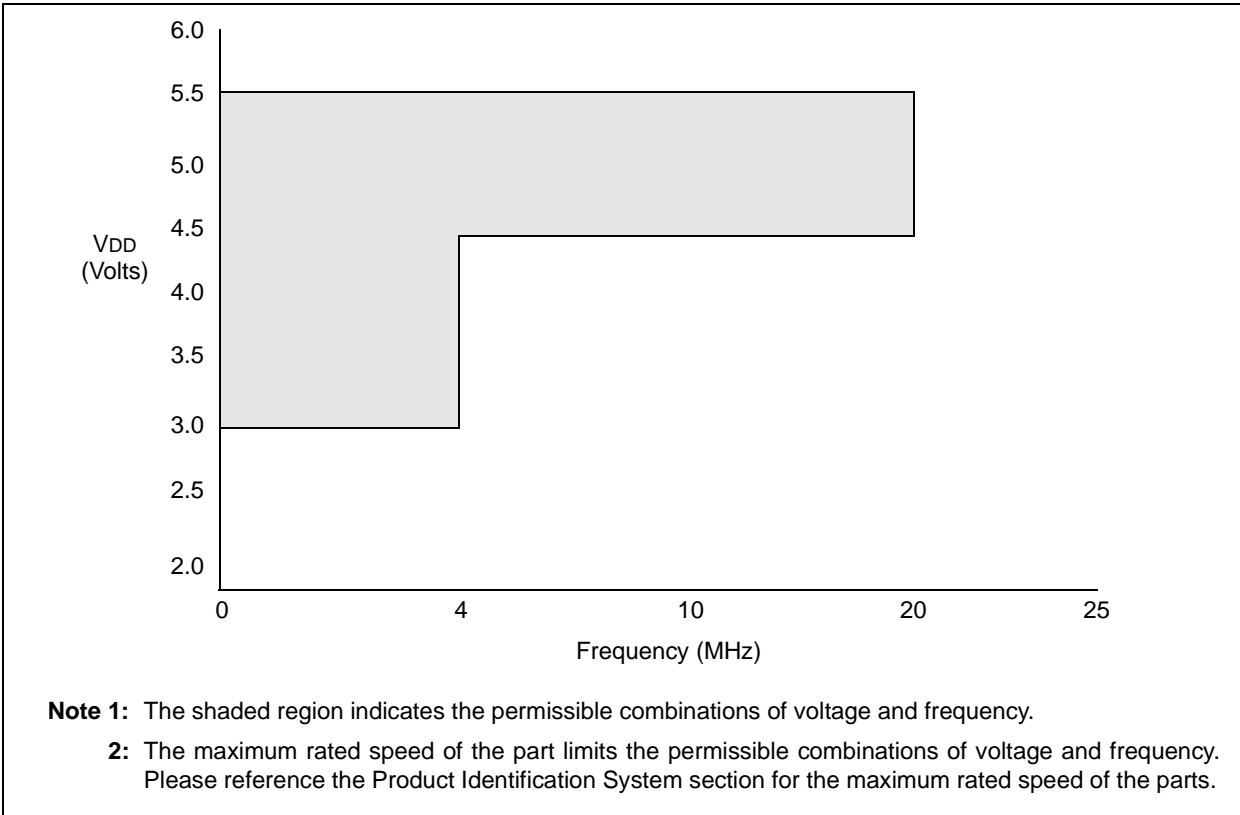
Legend: x = unknown, u = unchanged, - = unimplemented read as '0'. Shaded cells are not used by Capture and Timer1.

3. Valid regions of operation:

**FIGURE 17-1: PIC16F62X VOLTAGE-FREQUENCY GRAPH,  $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$**



**FIGURE 17-2: PIC16F62X VOLTAGE-FREQUENCY GRAPH,  $-40^{\circ}\text{C} \leq T_A < 0^{\circ}\text{C}$ ,  $+70^{\circ}\text{C} < T_A \leq +125^{\circ}\text{C}$**



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FIGURE 17-3: PIC16LF62X VOLTAGE-FREQUENCY GRAPH,  $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$

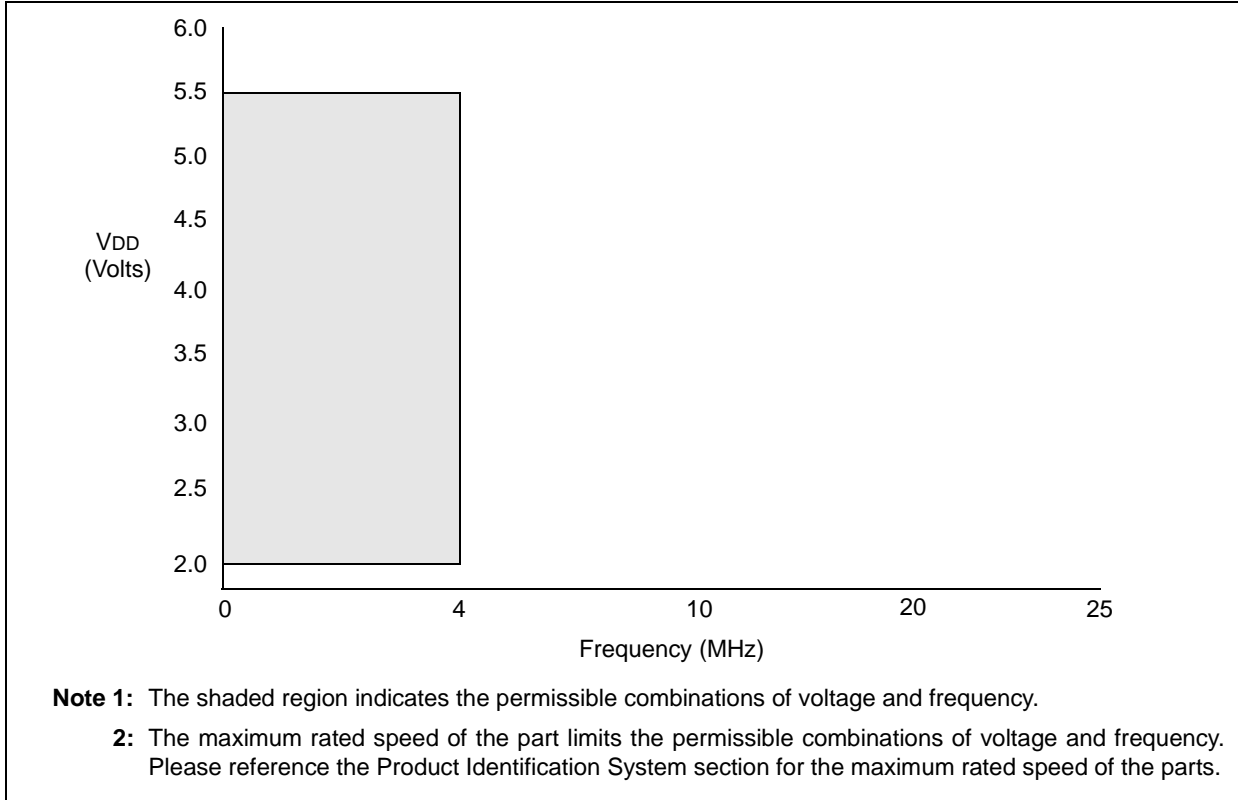
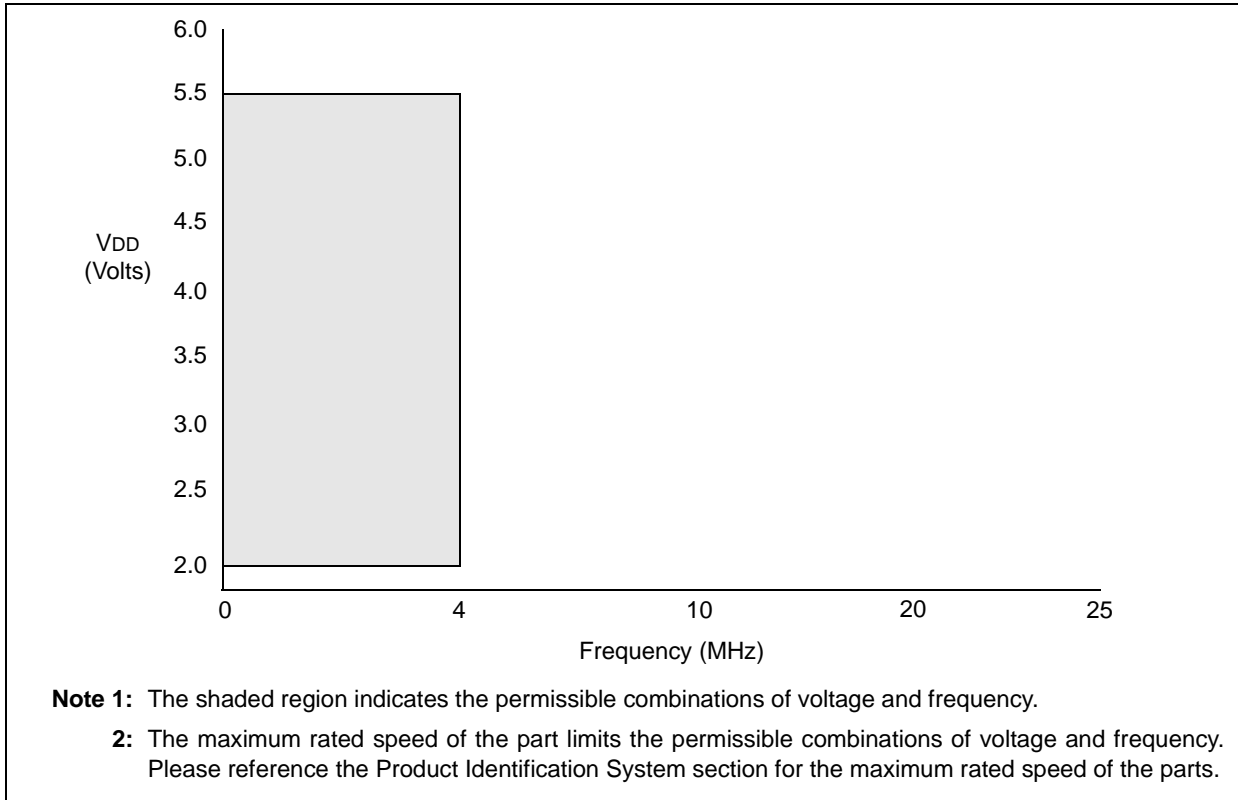


FIGURE 17-4: PIC16LF62X VOLTAGE-FREQUENCY GRAPH,  $+70^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$



**TABLE 17-1: DC CHARACTERISTICS: PIC16F62X-04 (COMMERCIAL, INDUSTRIAL, EXTENDED)  
PIC16F62X-20 (COMMERCIAL, INDUSTRIAL, EXTENDED)**

| Standard Operating Conditions (unless otherwise stated)<br>Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for industrial and<br>$0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$ for commercial and<br>$-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for extended |                    |   |       |      |      |       |  |
|--|--------------------|---|-------|------|------|-------|--|
| Param No.  | Sym                | Characteristic  | Min   | Typ† | Max  | Units | Conditions   |
| D001   | VDD                | Supply Voltage  | 3.0   | -    | 5.5  | V     |  |
| D002   | VDR                | RAM Data Retention Voltage (Note 1)   | -     | 1.5* | -    | V     | Device in SLEEP mode   |
| D003   | VPOR               | VDD start voltage to ensure Power-on Reset  | -     | VSS  | -    | V     | See section on power-on reset for details  |
| D004   | SVDD               | VDD rise rate to ensure Power-on Reset  | 0.05* | -    | -    | V/ms  | See section on power-on reset for details  |
| D005   | VBOD               | Brown-out Detect Voltage  | 3.7   | 4.0  | 4.35 | V     | BODEN configuration bit is cleared   |
| D010   | IDD                | Supply Current (Note 2, 5)  | -     | -    | 0.7  | mA    | FOSC = 4.0MHz, VDD = 3.0   |
| D013   |                    |   | -     | 4.0  | 7.0  | mA    | FOSC = 4.0MHz, VDD = 5.5*  |
|  |                    |   | -     | -    | 6.0  | mA    | FOSC = 20.0MHz, VDD = 5.5*   |
|  |                    |   | -     | -    | 2.0  | mA    | FOSC = 20.0MHz, VDD = 4.5<br>FOSC = 10.0MHz, VDD = 3.0 (Note 6)<br>FOSC = 32kHz, VDD = 3.0 |
| D020   | IPD                | Power Down Current (Note 3)   | -     | -    | 2.2  | μA    | VDD = 3.0  |
|  |                    |   | -     | -    | 5.0  | μA    | VDD = 4.5  |
|  |                    |   | -     | -    | 9.0  | μA    | VDD = 5.5*   |
|  |                    |   | -     | -    | 15.0 | μA    | VDD = 5.5 Extended*  |
| D022   | ΔI <sub>WDT</sub>  | WDT Current (Note 4)  | -     | 6.0  | 20   | μA    | VDD = 4.0V   |
| D022A  | ΔI <sub>BOD</sub>  | Brown-out Detect Current (Note 4)<br>Comparator Current for each<br>Comparator (Note 4) | -     | 75   | 125  | μA    | BOD enabled, VDD = 5.0V<br>VDD = 4.0V  |
| D023   | ΔI <sub>COMP</sub> |   | -     | 30   | 50   | μA    |  |
| D023A  | ΔI <sub>VREF</sub> |   | -     | -    | 135  | μA    |  |
| 1A   | FOSC               | LP Oscillator Operating Frequency   | 0     | -    | 200  | kHz   | All temperatures   |
|  |                    | INTRC Oscillator Operating Frequency  | -     | -    | 4    | MHz   | All temperatures   |
|  |                    | XT Oscillator Operating Frequency   | 0     | -    | 4    | MHz   | All temperatures   |
|  |                    | HS Oscillator Operating Frequency   | 0     | -    | 20   | MHz   | All temperatures   |

\* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C, unless otherwise stated. These parameters are for design guidance only and are not tested.

**Note 1:** This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

**2:** The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern and temperature also have an impact on the current consumption.

The test conditions for all IDD measurements in active operation mode are:

OSC1 = external square wave, from rail to rail; all I/O pins tri-stated, pulled to VDD,

MCLR = VDD; WDT enabled/disabled as specified.

**3:** The power down current in SLEEP mode does not depend on the oscillator type. Power down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD or VSS.

**4:** The Δ current is the additional current consumed when this peripheral is enabled. This current should be added to the base IDD or IPD measurement.

**5:** For RC osc configuration, current through Rext is not included. The current through the resistor can be estimated by the formula,  $I_r = VDD/2R_{ext}$  (mA) with Rext in kΩ.

**6:** Commercial temperature range only.

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**TABLE 17-2: DC CHARACTERISTICS: PIC16LF62X-04 (COMMERCIAL, INDUSTRIAL, EXTENDED)**

| Standard Operating Conditions (unless otherwise stated)   |                    |   |       |      |      |       |   |
|---|--------------------|---|-------|------|------|-------|---|
| Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for industrial and<br>$0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$ for commercial and<br>$-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for extended |                    |   |       |      |      |       |   |
| Operating voltage $V_{DD}$ range as described in DC spec Table 17-1 and Table 12-2  |                    |   |       |      |      |       |   |
| Param No.   | Sym                | Characteristic                                  | Min   | Typ† | Max  | Units | Conditions  |
| D001  | VDD                | Supply Voltage                                  | 2.0   | -    | 5.5  | V     |   |
| D002  | VDR                | RAM Data Retention Voltage (Note 1)             | -     | 1.5* | -    | V     | Device in SLEEP mode  |
| D003  | VPOR               | VDD start voltage to ensure Power-on Reset      | -     | VSS  | -    | V     | See section on Power-on Reset for details   |
| D004  | SVDD               | VDD rise rate to ensure Power-on Reset          | 0.05* | -    | -    | V/ms  | See section on Power-on Reset for details   |
| D005  | VBOD               | Brown-out Detect Voltage                        | 3.7   | 4.0  | 4.35 | V     | BODEN configuration bit is cleared  |
| D010  | IDD                | Supply Current (Note 2, 5)                      | -     | -    | 0.6  | mA    | FOSC = 4.0MHz, VDD = 2.0, WDT disabled (Note 5)   |
| D013  |                    |   |       |      |      |       | FOSC = 4.0MHz, VDD = 5.5, WDT disabled (Note 5)*<br>FOSC = 32kHz, VDD = 2.0, WDT disabled |
| D020  | IPD                | Power Down Current (Note 2, 3)                  | -     | -    | 2.0  | μA    | VDD = 2.0   |
|   |                    |   |       |      | 2.2  | μA    | VDD = 2.5*  |
|   |                    |   |       |      | 9.0  | μA    | VDD = 3.0*  |
|   |                    |   |       |      | 15.0 | μA    | VDD = 5.5<br>VDD = 5.5 Extended   |
| D023  | ΔI <sub>WDT</sub>  | WDT Current (Note 4)                            | -     | 6.0  | 15   | μA    | VDD = 3.0V  |
|   | ΔI <sub>BOD</sub>  | Brown-out Detect Current (Note 4)               | -     | 75   | 125  | μA    | BOD enabled, VDD = 5.0V   |
|   | ΔI <sub>COMP</sub> | Comparator Current for each Comparator (Note 4) | -     | 30   | 50   | μA    | VDD = 3.0V  |
|   | ΔI <sub>VREF</sub> | VREF Current (Note 4)                           | -     | -    | 135  | μA    | VDD = 3.0V  |
| 1A  | FOSC               | LP Oscillator Operating Frequency               | 0     | -    | 200  | kHz   | All temperatures  |
|   |                    | INTRC Oscillator Operating Frequency            | -     | -    | 4    | MHz   | All temperatures  |
|   |                    | XT Oscillator Operating Frequency               | 0     | -    | 4    | MHz   | All temperatures  |
|   |                    | HS Oscillator Operating Frequency               | 0     | -    | 20   | MHz   | All temperatures  |

\* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C, unless otherwise stated. These parameters are for design guidance only and are not tested.

**Note 1:** This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

**2:** The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern, and temperature also have an impact on the current consumption.

The test conditions for all IDD measurements in active operation mode are:

OSC1=external square wave, from rail to rail; all I/O pins tristated, pulled to VDD,

MCLR = VDD; WDT enabled/disabled as specified.

**3:** The power down current in SLEEP mode does not depend on the oscillator type. Power down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD to VSS.

**4:** The Δ current is the additional current consumed when this peripheral is enabled. This current should be added to the base IDD or IPD measurement.

**5:** For RC osc configuration, current through Rext is not included. The current through the resistor can be estimated by the formula  $I_r = V_{DD}/2R_{ext}$  (mA) with Rext in kΩ.

**TABLE 17-3: DC CHARACTERISTICS: PIC16F62X (COMMERCIAL, INDUSTRIAL, EXTENDED)  
PIC16LF62X (COMMERCIAL, INDUSTRIAL, EXTENDED)**

| Standard Operating Conditions (unless otherwise stated)   |          |   |                                   |      |                             |               |   |
|---|----------|---|-----------------------------------|------|-----------------------------|---------------|---|
| Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for industrial and<br>$0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$ for commercial and<br>$-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for extended |          |   |                                   |      |                             |               |   |
| Operating voltage $V_{DD}$ range as described in DC spec Table 17-1 and Table 12-2  |          |   |                                   |      |                             |               |   |
| Param. No.  | Sym      | Characteristic  | Min                               | Typ† | Max                         | Unit          | Conditions  |
| D030  | $V_{IL}$ | <b>Input Low Voltage</b><br>I/O ports<br>with TTL buffer      | $V_{SS}$                          | –    | 0.8V<br>0.15V <sub>DD</sub> | V             | $V_{DD} = 4.5\text{V to } 5.5\text{V}$<br>otherwise                                     |
| D031  |          | with Schmitt Trigger input                                    | $V_{SS}$                          | –    | 0.2V <sub>DD</sub>          | V             | Note1   |
| D032  |          | $\overline{\text{MCLR}}$ , RA4/T0CKI, OSC1 (in ER mode)       | $V_{SS}$                          | –    | 0.2V <sub>DD</sub>          | V             |   |
| D033  |          | OSC1 (in XT and HS)   | $V_{SS}$                          | –    | 0.3V <sub>DD</sub>          | V             |   |
|   |          | OSC1 (in LP)  | $V_{SS}$                          | –    | 0.6V <sub>DD</sub> -1.0     | V             |   |
| D040  | $V_{IH}$ | <b>Input High Voltage</b><br>I/O ports<br>with TTL buffer     | 2.0V<br>.25V <sub>DD</sub> + 0.8V | –    | $V_{DD}$<br>$V_{DD}$        | V             | $V_{DD} = 4.5\text{V to } 5.5\text{V}$<br>otherwise                                     |
| D041  |          | with Schmitt Trigger input                                    | 0.8V <sub>DD</sub>                | –    | $V_{DD}$                    | V             |   |
| D042  |          | $\overline{\text{MCLR}}$ RA4/T0CKI                            | 0.8V <sub>DD</sub>                | –    | $V_{DD}$                    | V             |   |
| D043  |          | OSC1 (XT, HS and LP)  | 0.7V <sub>DD</sub>                | –    | $V_{DD}$                    | V             |   |
| D043A   |          | OSC1 (in ER mode)   | 0.9V <sub>DD</sub>                | –    |                             |               | Note1   |
| D070  | IPURB    | PORTB weak pull-up current                                    | 50                                | 200  | 400                         | $\mu\text{A}$ | $V_{DD} = 5.0\text{V}$ , $V_{PIN} = V_{SS}$   |
|   |          | <b>Input Leakage Current</b><br>(Notes 2, 3)                  |                                   |      |                             |               |   |
| D060  | $I_{IL}$ | I/O ports (Except PORTA)                                      | –                                 | –    | $\pm 1.0$                   | $\mu\text{A}$ | $V_{SS} \leq V_{PIN} \leq V_{DD}$ , pin at hi-impedance                                 |
| D061  |          | PORTA   | –                                 | –    | $\pm 0.5$                   | $\mu\text{A}$ | $V_{SS} \leq V_{PIN} \leq V_{DD}$ , pin at hi-impedance                                 |
| D063  |          | RA4/T0CKI   | –                                 | –    | $\pm 1.0$                   | $\mu\text{A}$ | $V_{SS} \leq V_{PIN} \leq V_{DD}$   |
|   |          | OSC1, $\overline{\text{MCLR}}$                                | –                                 | –    | $\pm 5.0$                   | $\mu\text{A}$ | $V_{SS} \leq V_{PIN} \leq V_{DD}$ , XT, HS and LP osc configuration                     |
| D080  | $V_{OL}$ | <b>Output Low Voltage</b><br>I/O ports                        | –                                 | –    | 0.6                         | V             | $I_{OL}=8.5\text{ mA}$ , $V_{DD}=4.5\text{V}$ , $-40^{\circ}$ to $+85^{\circ}\text{C}$  |
| D083  |          | OSC2/CLKOUT (ER only)   | –                                 | –    | 0.6                         | V             | $I_{OL}=7.0\text{ mA}$ , $V_{DD}=4.5\text{V}$ , $+125^{\circ}\text{C}$                  |
|   |          |   | –                                 | –    | 0.6                         | V             | $I_{OL}=1.6\text{ mA}$ , $V_{DD}=4.5\text{V}$ , $-40^{\circ}$ to $+85^{\circ}\text{C}$  |
|   |          |   | –                                 | –    | 0.6                         | V             | $I_{OL}=1.2\text{ mA}$ , $V_{DD}=4.5\text{V}$ , $+125^{\circ}\text{C}$                  |
| D090  | $V_{OH}$ | <b>Output High Voltage</b> (Note 3)<br>I/O ports (Except RA4) | $V_{DD}-0.7$                      | –    | –                           | V             | $I_{OH}=-3.0\text{ mA}$ , $V_{DD}=4.5\text{V}$ , $-40^{\circ}$ to $+85^{\circ}\text{C}$ |
| D092  |          | OSC2/CLKOUT (ER only)   | $V_{DD}-0.7$                      | –    | –                           | V             | $I_{OH}=-2.5\text{ mA}$ , $V_{DD}=4.5\text{V}$ , $+125^{\circ}\text{C}$                 |
|   |          |   | $V_{DD}-0.7$                      | –    | –                           | V             | $I_{OH}=-1.3\text{ mA}$ , $V_{DD}=4.5\text{V}$ , $-40^{\circ}$ to $+85^{\circ}\text{C}$ |
|   |          |   | $V_{DD}-0.7$                      | –    | –                           | V             | $I_{OH}=-1.0\text{ mA}$ , $V_{DD}=4.5\text{V}$ , $+125^{\circ}\text{C}$                 |
| *D150   | $V_{OD}$ | <b>Open-Drain High Voltage</b>                                |                                   | –    | 8.5*                        | V             | RA4 pin PIC16F62X, PIC16LF62X   |
|   |          | <b>Capacitive Loading Specs on Output Pins</b>                |                                   |      |                             |               |   |
| D100  | COSC2    | OSC2 pin  |                                   | –    | 15                          | pF            | In XT, HS and LP modes when external clock used to drive OSC1.                          |
| D101  | CIO      | All I/O pins/OSC2 (in ER mode)                                |                                   | –    | 50                          | pF            |   |

\* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**Note 1:** In ER oscillator configuration, the OSC1 pin is a Schmitt Trigger input. It is not recommended that the PIC16F62X be driven with external clock in ER mode.

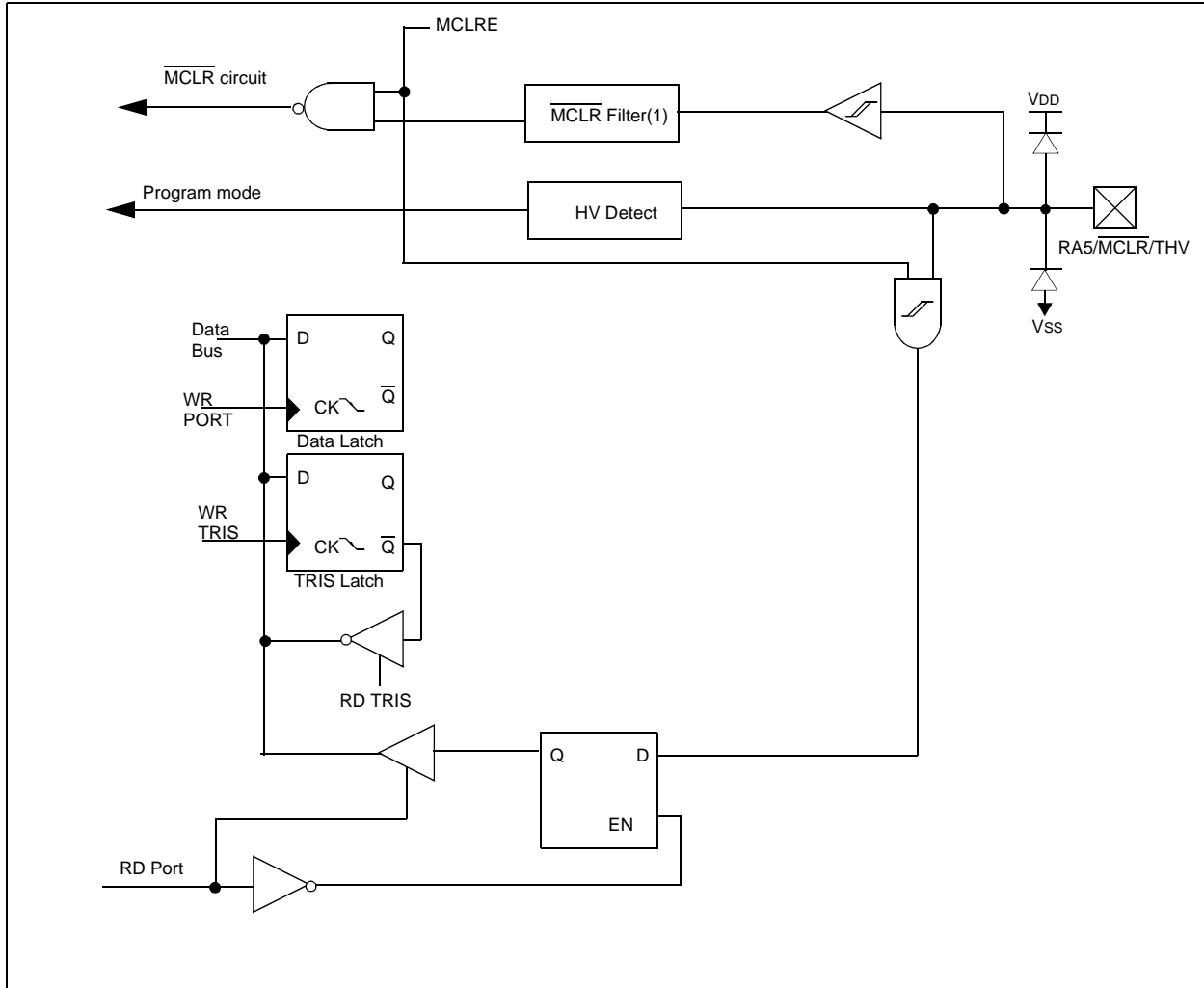
**2:** The leakage current on the  $\overline{\text{MCLR}}$  pin is strongly dependent on applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

**3:** Negative current is defined as coming out of the pin.

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4. The following block diagram shown in Section 5, Figure 5-5 is incorrect. The following figure should be used instead.

**FIGURE 5-5: BLOCK DIAGRAM OF THE RA5/MCLR/THV PIN**





5. The example given in Section 9, Example 9-1, concerning Initializing the Comparator Module is incorrect. The following code example should be used instead.

## EXAMPLE 9-1: INITIALIZING COMPARATOR MODULE

```
BCF      INTCON,GIE      ; Turn OFF Global Interrupts
BCF      INTCON,PEIE     ; Turn OFF Peripheral Interrupts
CLRF     PORTA          ; Init Port A
MOVLW   0X03            ; Init comparator mode
MOVWF   CMCON           ; CM<2:0> = 011
BSF     STATUS,RP0      ; Select BANK 1
MOVLW   0x07            ; Initialize Port A Direction
MOVWF   TRISA           ; Set RA<2:0> as Inputs
                          ; RA<4:3> as outputs
                          ; TRIS<5> always reads '0'

BCF     STATUS,RP0      ; Select BANK 0
CALL    DELAY10         ; Wait 10us for comparator output to become valid
                          ; See Table 17-1 Parameter 301

MOVF    CMCON,F         ; Read CMCON to end change condition
BCF     PIR1,CMIF       ; Clear pending interrupts
BSF     STATUS,RP0      ; Select BANK 1
BSF     PIE1,CMIE       ; Enable Comparator Interrupts
BCF     STATUS,RP0      ; Select BANK 0
BSF     INTCON,PEIE     ; Enable Peripheral Interrupts
BSF     INTCON,GIE      ; Global Interrupt Enable

; Insert Your code....

; Helper function is the Delay for 10us routine show below.

DELAY10      ; burns 8 cycles + the call for 10 cycles or 10us at 4Mhz
goto $+1     ; goto the next instruction and burn 2 cycles
call retlbl  ; goto the next instruction and burn 2 more cycles
retlbl return ; go back and burn 2 cycles (actually done 2x for 4 cycles consumed)
```

# PIC16F627

---

6. The examples given in Section 13, concerning the Data EEPROM are incorrect. The EEPROM registers are all located in Bank 1. The examples show the registers in Bank 0 and Bank 1. The following code examples should be used instead to use this feature.

## EXAMPLE 13-1: DATA EEPROM READ

```
BSF     STATUS, RP0 ; Bank 1
MOVLW  CONFIG_ADDR ;
MOVWF  EEADR       ; Address to read
BSF     EECON1, RD  ; EE Read
MOVF   EEDATA, W   ; W = EEDATA
BCF     STATUS, RP0 ; Bank 0
```

## EXAMPLE 13-2: DATA EEPROM WRITE

```
                ; set up the data and
                ; the address
BSF     STATUS, RP0 ; Bank 1
MOVLW  CONFIG_ADDR ;
MOVWF  EEADR       ; Address to write
MOVLW  CONFIG_DATA ;
MOVWF  EEDATA      ; Data to write

                ; perform the write
                ; operation
BSF     EECON, WREN ; Enable Write
BCF     INTCON, GIE ; Disable INTs
MOVLW  055h       ;
MOVWF  EECON2     ; Write 55
MOVLW  0AAh       ;
MOVWF  EECON2     ; Write AA
BSF     EECON1, WR ; Set WR bit
BCF     STATUS, RP0 ; Bank 0
```

## EXAMPLE 13-3: DATA EEPROM VERIFY

```
; after the write is complete (i.e. in the
write interrupt)
BSF     STATUS, RP0 ; Bank 1
MOVF   EEDATA, W   ; load the last
                    ; written value into W
BSF     EECON, RD  ; start a read
;
; Is the value written (in W Reg) and
; read (in EEDATA) the same?
;
SUBWF  EEDATA, W   ; the EEDATA has fresh
                    ; data
BTFSS  STATUS, Z   ; Is the Zero flag set?
GOTO   WRITE_ERR   ; NO, Write Error
                    ; YES, Good Write
                    ; continue program
```

NOTES:



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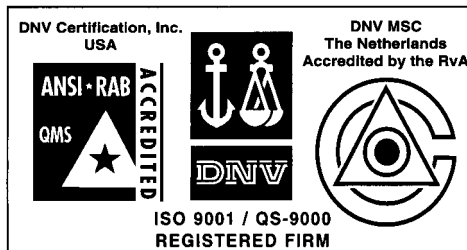
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